

Figure 1

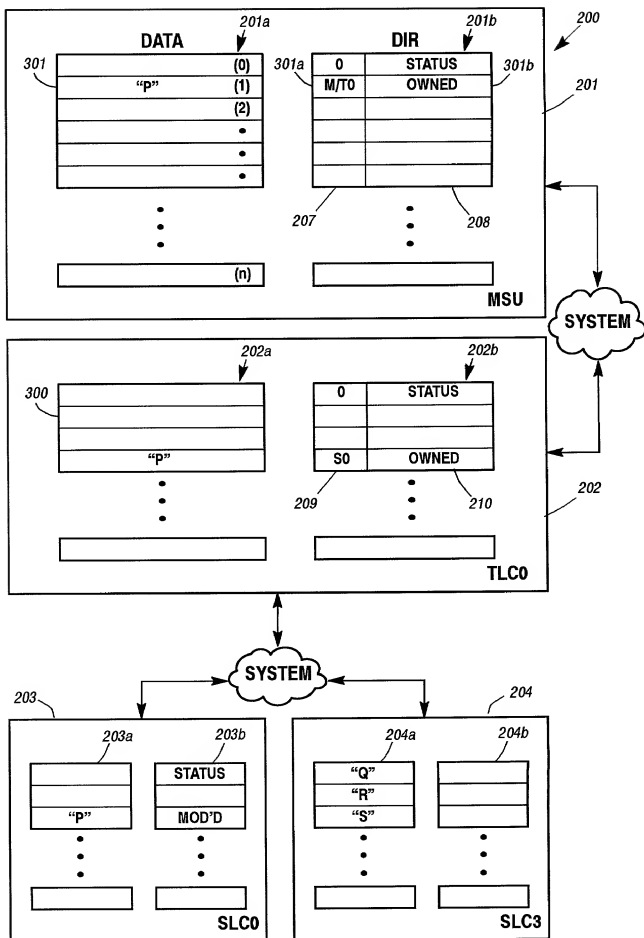


Figure 2

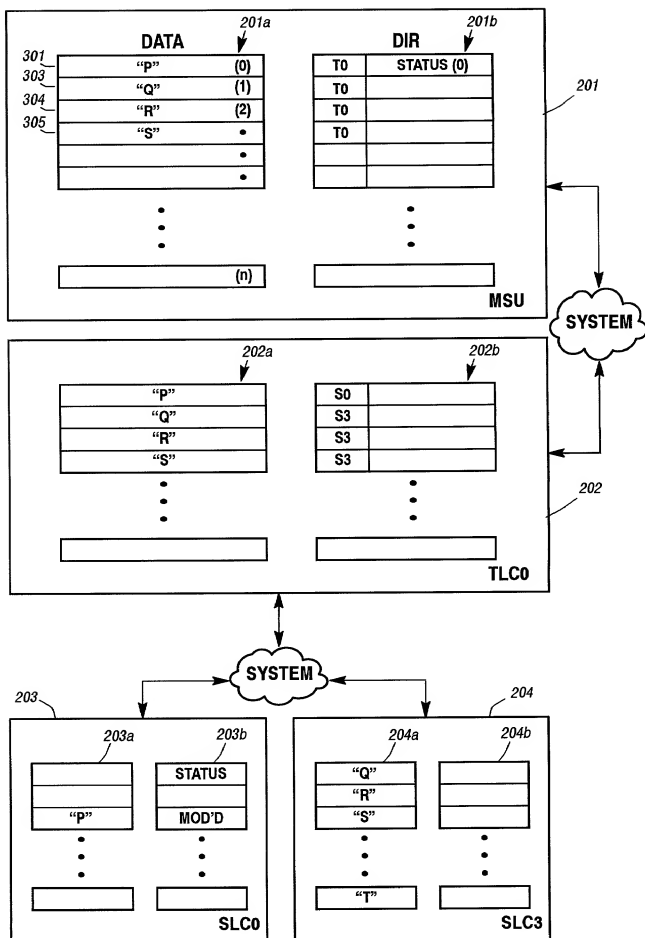


Figure 2A

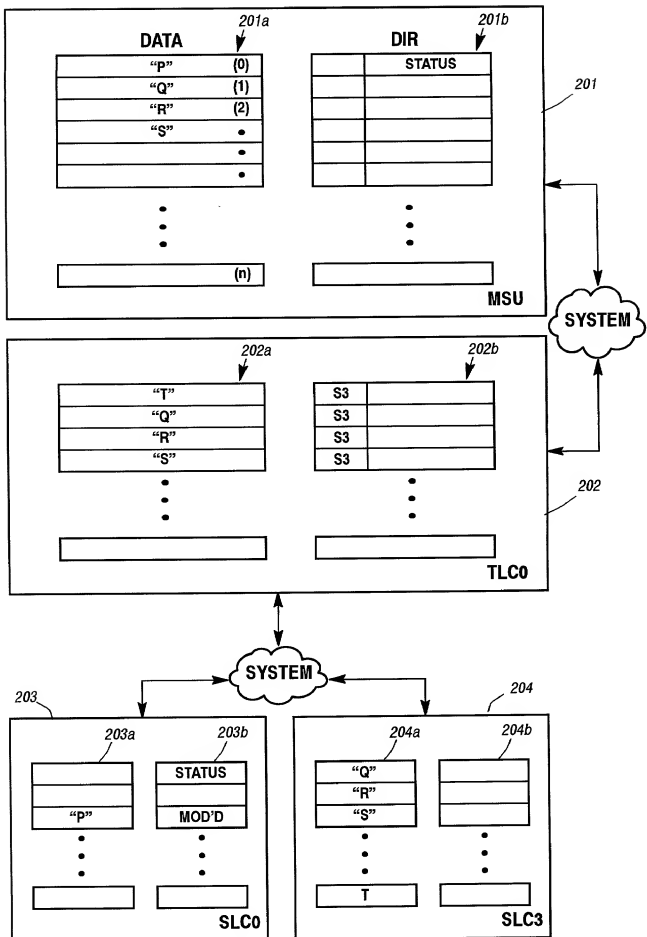


Figure 2B

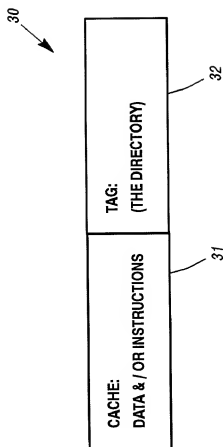


Figure 3

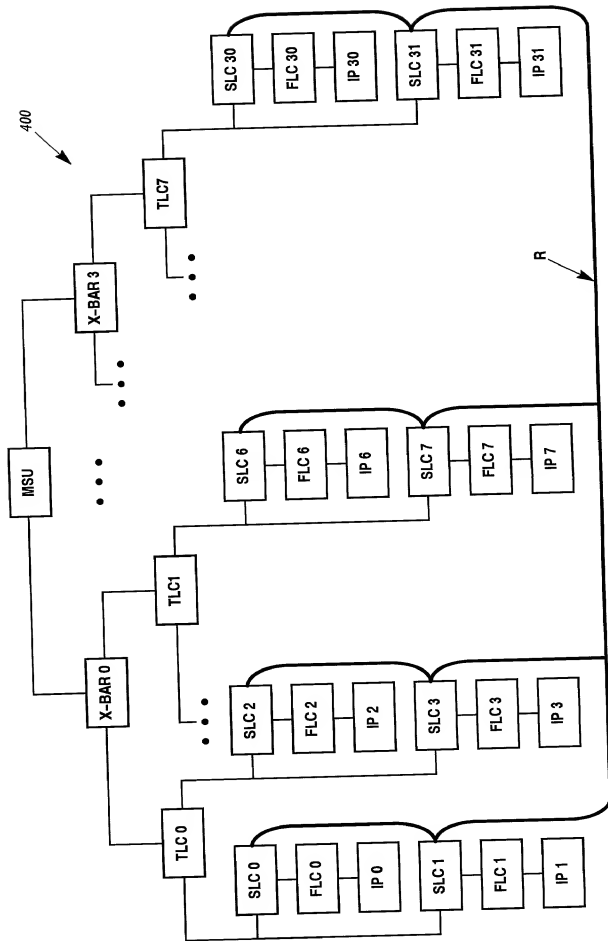


Figure 4

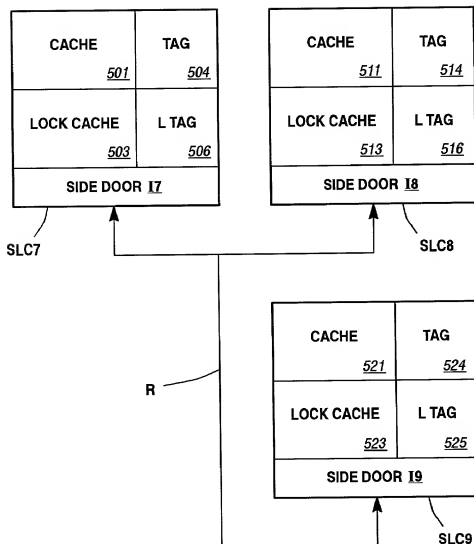


Figure 5

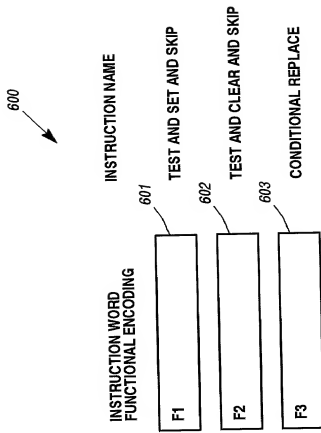


Figure 6
Lock Instructions

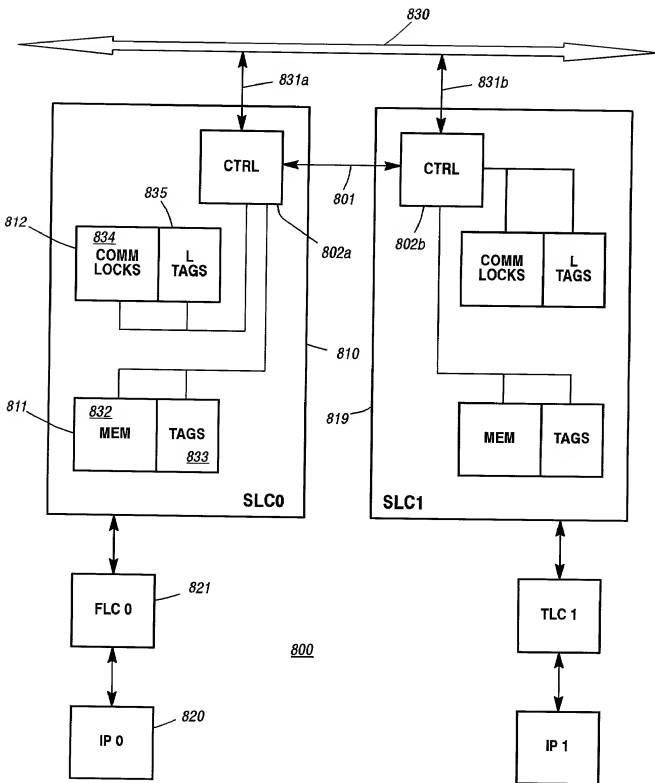


Figure 8A

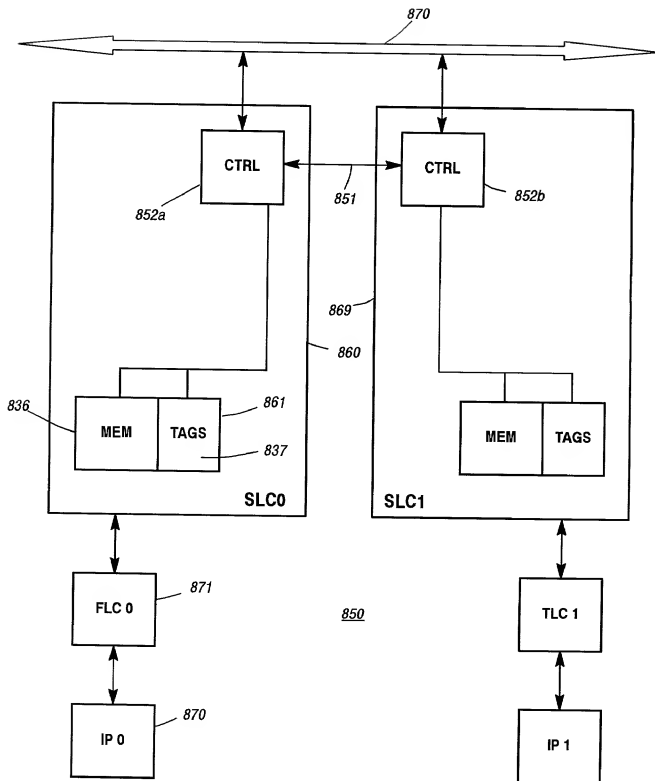


Figure 8B

700

ADDR 1	SLC 0
ADDR 2	SLC 0
•	SLC 7
•	SLC 7
•	SLC 15
	SLC 6
ADDR X	SLC 8
•	SLC 9
•	SLC 0
•	SLC 9
	SLC 32
ADDR n	SLC 32

902

901
(LD7)

900
(SLC 7
COM-LOCK
MEM
ARRAY)

Figure 9

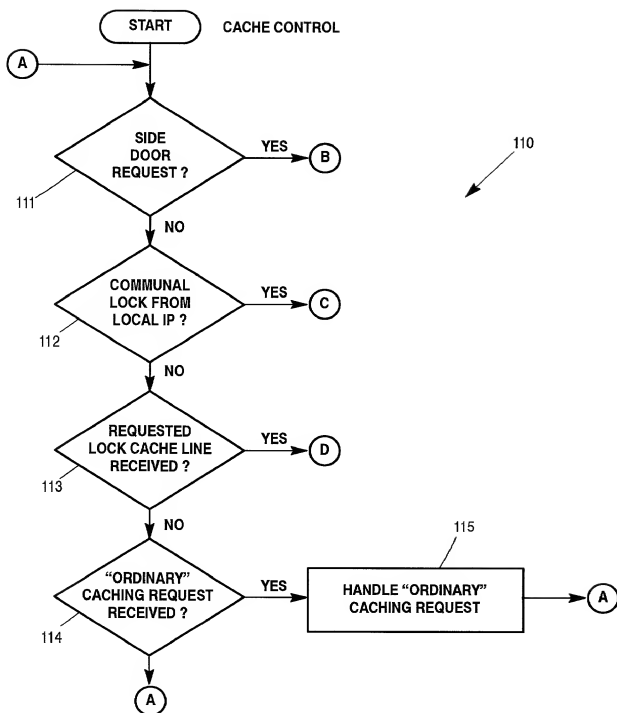


Figure 10A

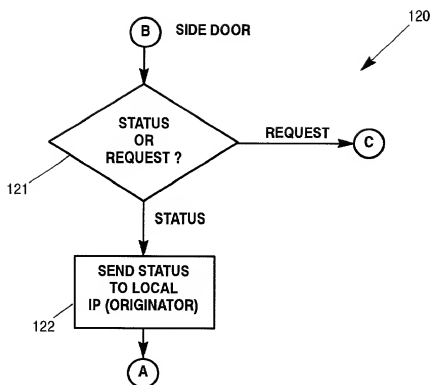


Figure 10B

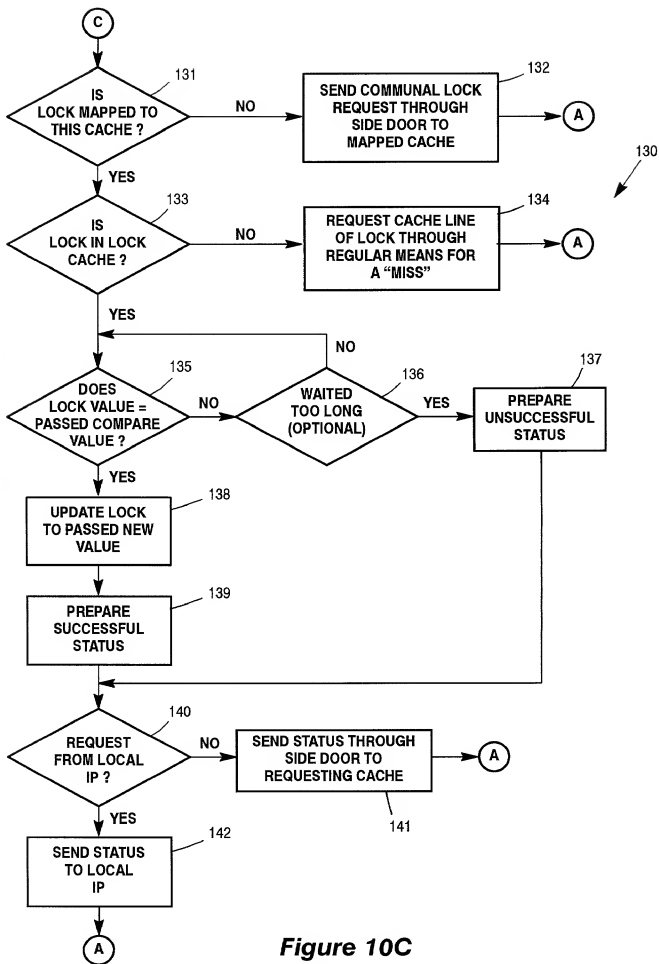


Figure 10C

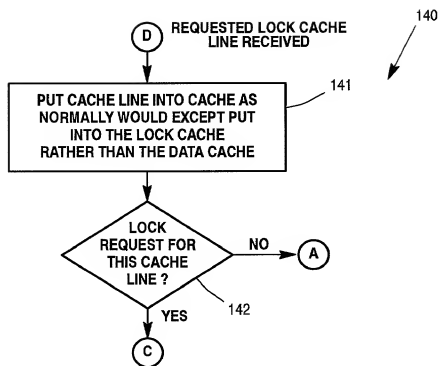


Figure 10D

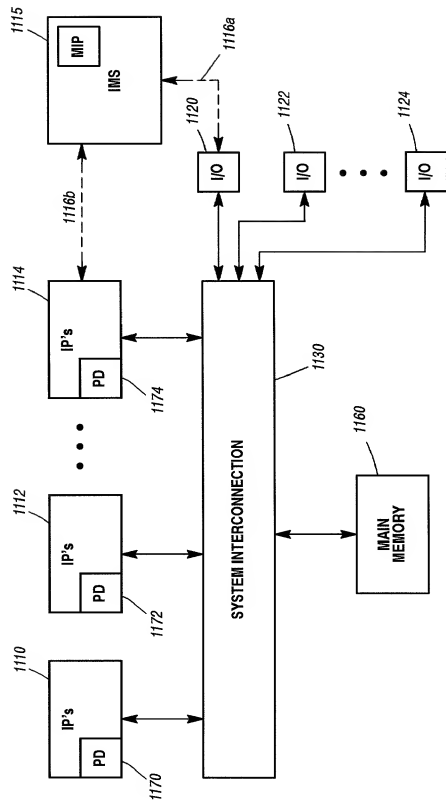


Figure 11

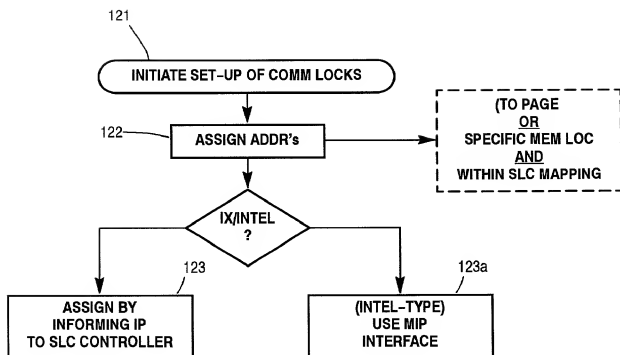
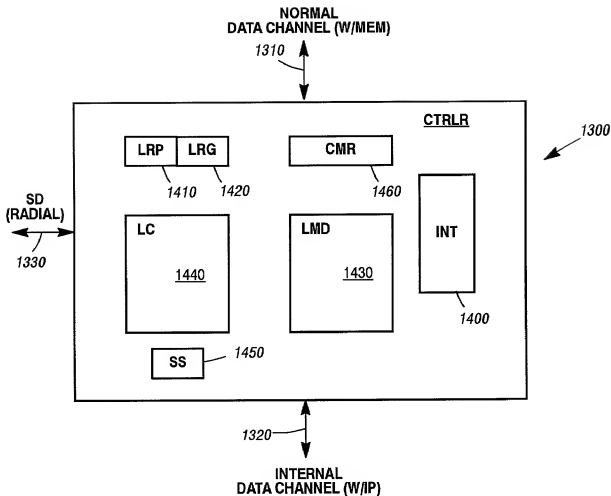


Figure 12



- LRG = LOCK REQ. GENERATOR - GENERATES / FORWARDS LOCK REQUEST IF LRP SAYS IT D/N HAVE IT.
 LRP = LOCK REQUEST (INSTRUCTION) PROCESSOR (HAS BIT CHANGER & CHECKS LMD & LC TO SEE IF (A) IT'S HIS & (B) IF HE HAS IT)
 SD = SIDE DOOR (INCLUDES ID INFO PATH)
 CMR = COMPARATOR
 LMD = LOCK MAP DIRECTORY
 LC = LOCK CACHE
 INT = INTERPRETER (IS THIS A LOCK REQUEST? ELSE PASS THROUGH AS NORMAL DATA)
 SS = STATUS STRIPPER (SENDS BACK LOCK STATUS TO SIDE DOOR WHEN OPERATION COMPLETES IN RESP TO SIDE DOOR REQ)

Figure 13